CLAIMS

1. Single cell erasing method for recovering memory cells under reading or programming disturbs, in non volatile semiconductor memory electronic devices comprising cell matrix split in sectors and organized in rows, or word line, and columns, or bit lines, of the type providing the application of a sector erasing algorithm with subsequent testing phase (erase-verify), characterised in that it provides a bit by bit erasing by applying to each single word line a negative voltage used during the erasing of a whole sector and on the drain terminal of each single cell a programming voltage.

2. Method according to claim 1, characterised in that it is applied to cells having a higher threshold than the original one.

3. Method according to claim 1, characterised in that it provides also a bias to a negative voltage value of the cell substrate or of the cell bulk terminal.

4. Method according to claim 1, characterised in that it provides initially a search phase of which cells have a higher threshold voltage than the original value and a subsequent application phase of said bit by bit erasing.

5. Method according to claim 1, characterised in that a subsequent erase-verify phase is performed after the bit by bit erasing.

6. Method according to claim 1, characterised in that said cell matrix is a Page-Flash array.

7. A method of erasing individual flash memory cells contained in an array of flash memory cells, the array being arranged in sectors with each sector including a portion of the memory cells contained in the array, each flash memory cell having a control terminal coupled to a word line and a drain terminal coupled to a bit line, the method comprising:

applying a negative programming voltage on a selected word line of a sector of memory cells; and

applying a positive voltage on a selected bit line of the sector of memory cells.

8. The method of claim 7 further comprising:

determining which memory cells in the sector have a threshold voltage greater than a threshold value; and

performing the operations of applying on all memory cells in the sector determined to have threshold voltages greater than the threshold value.

9. The method of claim 8 wherein determining which memory cells in the sector have a threshold voltage greater than the threshold value comprises:

applying to each memory cell determined to have a threshold voltage greater than the threshold value a test voltage having a value equal to an erase-verify voltage plus a voltage margin.

10. The method of claim 8 further comprising:

verifying a memory cell receiving the applied voltages on the word and bit lines has been properly erased after the operations of applying have been performed on the memory cell.

11. The method of claim 7 further comprising maintaining the other bit lines associated with the sector at ground.

12. The method of claim 7 further comprising performing a block erase of all memory cells in the sector prior to the operations of applying.

13. A flash memory device including a memory-cell array, the memory cell array being arranged in sectors with each sector including a portion of the memory cells contained in the array, each flash memory cell in the array having a control terminal coupled to a word line and a drain terminal coupled to a bit line, the memory device being operable to erase selected memory cells in a sector by applying a negative

programming voltage on a selected word line of the sector and applying a positive voltage on a selected bit line of the sector of memory cells.

14. The flash memory device of claim 13 wherein the memory-cell array comprises a page-flash array.

15. The flash memory device of claim 13 wherein the memory device is further operable to determine which memory cells in the sector have a threshold voltage greater than a threshold value and to apply the negative programming voltage and positive voltage to all memory cells in the sector determined to have threshold voltages greater than the threshold value.

16. The flash memory device of claim 15 wherein the memory device is further operable to apply to each memory cell determined to have a threshold voltage greater than the threshold value a test voltage having a value equal to an erase-verify voltage plus a voltage margin.

17. An electronic system, comprising:

a flash memory device, including,

a memory-cell array, the memory cell array being arranged in sectors with each sector including a portion of the memory cells contained in the array, each flash memory cell in the array having a control terminal coupled to a word line and a drain terminal coupled to a bit line, the memory device being operable to erase selected memory cells in a sector by applying a negative programming voltage on a selected word line of the sector and applying a positive voltage on a selected bit line of the sector of memory cells.

18. The electronic system of claim 17 wherein the system comprises a computer system.

19. The electronic system of claim 17 wherein the memory-cell array comprises

a page-flash array.

20. The electronic system of claim 17 wherein the memory device is further operable to determine which memory cells in the sector have a threshold voltage greater than a threshold value and to apply the negative programming voltage and positive voltage to all memory cells in the sector determined to have threshold voltages greater than the threshold value.